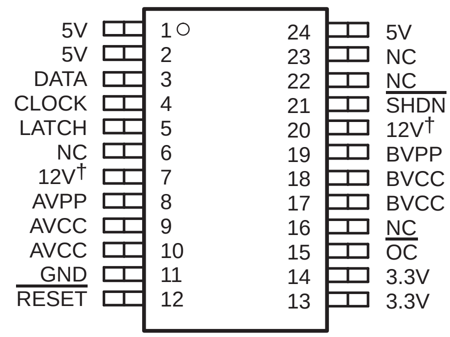
FEATURES

- Single-Slot Switch: SNP1x11
  Dual-Slot Switches: SNP2x31, SNP2x41, SNP2x61
- Fast Current Limit Response Time
- Fully Integrated VCC and VPP Switching for 3.3 V, 5 V, and 12 V (no 12 V on SNP2x31)
- Meets Current PC Card™ Standards
- V_{pp} Output Selection Independent of V_{CC}
- 12-V and 5-V Supplies Can Be Disabled
- TTL-Logic Compatible Inputs
- Short-Circuit and Thermal Protection
- 24-Pin HTSSOP, 24- or 30-Pin SSOP
- 140-μA (Typical) Quiescent Current from 3.3-V Input
- Break-Before-Make Switching
- Power-On Reset
- −40°C to 85°C Operating Ambient Temperature Range

APPLICATIONS

- Notebook and Desktop Computers
- Bar Code Scanners
- Digital Cameras
- Set-Top Boxes
- PDAs

SNP2x31, SNP2x41
DB OR PWP PACKAGE
(TOP VIEW)



NC − No internal connection

† Pin 7 and 20 are NC for SNP2x31.

DESCRIPTION

The SNP2x31, SNP2x41, and SNP2x61 CardBus™ power-interface switches provide an integrated power-management solution for two PC Card sockets. The SNP1x21 is a single-slot option for this family of devices. These devices allow the controlled distribution of 3.3 V, 5 V, and 12 V to each card slot. The current-limiting and thermal-protection features eliminate the need for fuses. Current-limit reporting helps the user isolate a system fault. The switch $r_{DS(on)}$ and current-limit values have been set for the peak and average current requirements stated in the PC Card specification, and optimized for cost.

This family of devices support independent VPP/VCC switching. A shutdown mode is supported independently on $\overline{SHDN}$ as well as in the serial interface. Optimized for lower power implementation, the SNP2x31 does not support 12-V switching to VPP.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES				
	PLASTIC SMALL OUTLINE			PowerPAD™ PLASTIC SMALL OUTLINE (PWP-24)†	
	DB-24		DB-30		
−40°C to 85°C	SNP2x31DB, SNP2x41DB	SNP1x21DB	SNP2x61DB	SNP2x31PWP, SNP2x41PWP	SNP1x21PWP

† The DB and PWP packages are also available taped and reeled. Add R suffix to device type (e.g., SNP2x31PWPR) for taped and reeled.

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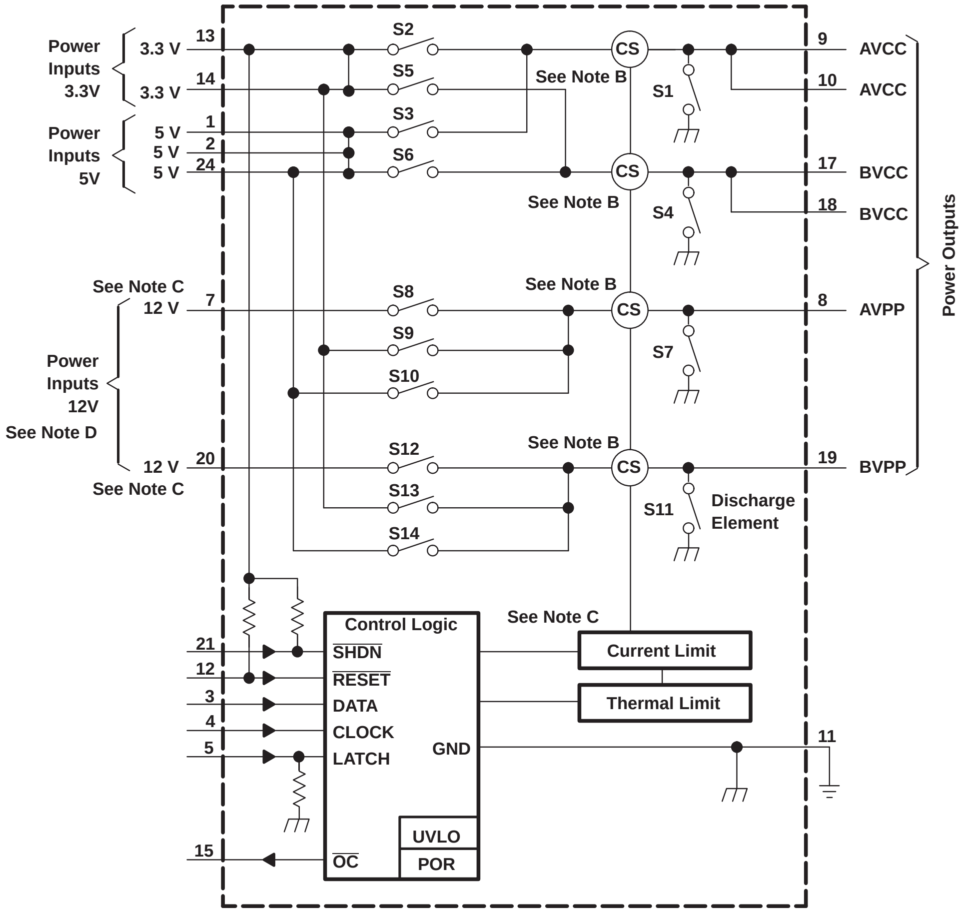
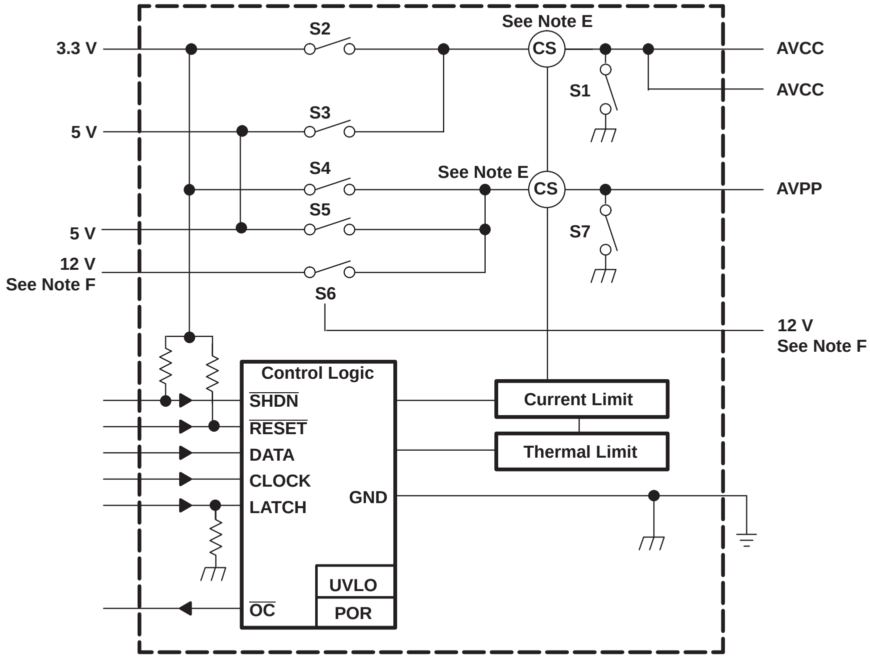
functional block diagram of SNP2x31, SNP2x41 SNP2x61 (See Note A)



NOTES: A. Diagram shown for 24-pin DB package.
B. Current sense
C. The two 12-V pins must be externally connected.
D. No connections for SNP2x31.

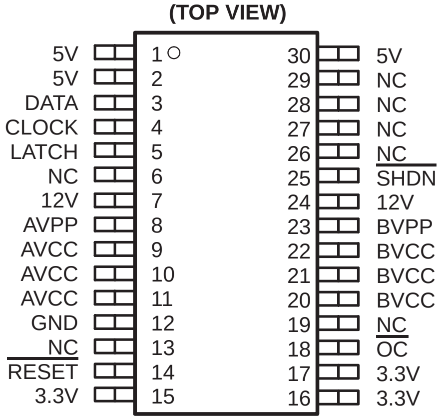
functional block diagram of SNP1x21



NOTES: E. Current sense
F. The two 12-V pins must be externally connected.

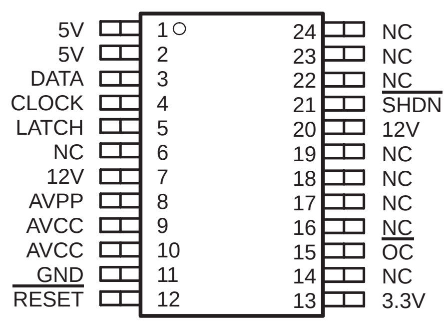
pin assignments

SNP2x61
DB PACKAGE
(TOP VIEW)



NC − No internal connection

SNP1x21
DB OR PWP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL					I/O	DESCRIPTION
NAME	NO.					
	SNP1X21	SNP2X31	SNP2X41	SNP2X61		
3.3V	13	13, 14	13, 14	15, 16, 17	I	3.3-V input for card power and chip power
5V	1, 2	1, 2, 24	1, 2, 24	1, 2, 30	I	5-V input for card power
12V	7, 20	NA	7, 20	7, 24	I	12-V input for card power (xVPP). The two 12-V pins must be externally connected.
AVCC	9, 10	9, 10	9, 10	9, 10, 11	O	Switched output that delivers 3.3 V, 5 V, ground or high impedance to card
AVPP	8	8	8	8	O	Switched output that delivers 3.3 V, 5 V, 12 V, ground or high impedance to card (12 V not applicable to SNP2x31)
BVCC	−−	17, 18	17, 18	20, 21, 22	O	Switched output that delivers 3.3 V, 5 V, ground or high impedance to card
BVPP	−−	19	19	23	O	Switched output that delivers 3.3 V, 5 V, 12 V, ground or high impedance to card (12 V not applicable for SNP2x31)
GND	11	11	11	12		Ground
$\overline{\text{OC}}$	15	15	15	18	O	Open-drain overcurrent reporting output that goes low when an overcurrent condition exists. An external pullup is required.
$\overline{\text{SHDN}}$	21	21	21	25	I	Hi-Z (open) all switches. Identical function to serial D8. Asynchronous active-low command, internal pullup
$\overline{\text{RESET}}$	12	12	12	14	I	Logic-level RESET input active low. Asynchronous active-low command, internal pullup
CLOCK	4	4	4	4	I	Logic-level clock for serial data word
DATA	3	3	3	3	I	Logic-level serial data word
LATCH	5	5	5	5	I	Logic-level latch for serial data word, internal pulldown
NC	6, 14, 16, 17, 18, 19, 22, 23, 24	6, 7, 16, 20, 22, 23	6, 16, 22, 23	6, 13, 19, 26, 27, 28, 29		No internal connection

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range for card power: $V_{I(3.3V)}$ . . . −0.3 V to 5.5 V
$V_{I(5V)}$ . . . −0.3 V to 5.5 V
$V_{I(12V)}$‡ . . . −0.3 V to 14 V
Logic input/output voltage . . . −0.3 V to 6 V
Output voltage: $V_{O(xVCC)}$ . . . −0.3 V to 6 V
$V_{O(xVPP)}$ . . . −0.3 V to 14 V
Continuous total power dissipation . . . See Dissipation Rating Table
Output current: $I_{O(xVCC)}$ . . . Internally Limited
$I_{O(xVPP)}$ . . . Internally Limited
Operating virtual junction temperature range, T_J . . . −40°C to 100°C
Storage temperature range, T_{STG} . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds) . . . 260°C
$\overline{OC}$ sink current . . . 10 mA

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Not applicable for SNP2x31

DISSIPATION RATING TABLE

PACKAGE§		$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	24	890 mW	8.9 mW/°C	489 mW	356 mW
	30	1095 mW	10.95 mW/°C	602 mW	438 mW
PWP	24	3322 mW	33.22 mW/°C	1827 mW	1329 mW

§ These devices are mounted on an JEDEC low-k board (2-oz. traces on surface).

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, $V_{I(3.3V)}$ is required for all circuit operations. 5V and 12V are only required for their respective functions.	$V_{I(3.3V)}$¶	3	3.6	V
	$V_{I(5V)}$	3	5.5	
	$V_{I(12V)}$‡	7	13.5	
Output current, I_O	$I_{O(xVCC)}$ at T_J = 100°C		1	A
	$I_{O(xVPP)}$ at T_J = 100°C		100	mA
Clock frequency, $f_{(clock)}$			2.5	MHz
Pulse duration, t_w	Data	200		ns
	Latch	250		
	Clock	100		
	Reset	100		
Data-to-clock hold time, t_h (see Figure 2)		100		ns
Data-to-clock setup time, t_{su} (see Figure 2)		100		ns
Latch delay time, $t_{d(latch)}$ (see Figure 2)		100		ns
Clock delay time, $t_{d(clock)}$ (see Figure 2)		250		ns
Operating virtual junction temperature, T_J (maximum to be calculated at worst case P_D at 85°C ambient)		−40	100	°C

‡ Not applicable for SNP2x31
¶ It is understood that for $V_{I(3.3V)} < 3$ V, voltages within the absolute maximum ratings applied to pin 5V or pin 12V do not damage the IC.

electrical characteristics, T_J = 25°C, $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V (not applicable for SNP2x31), all outputs unloaded (unless otherwise noted)

power switch

PARAMETER				TEST CONDITIONS†		MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance	3.3V to xVCC, (see Note 1)		I_O = 750 mA each			85	110	mΩ
				I_O = 750 mA each, T_J = 100°C			110	140	
		5V to xVCC, (see Note 1)		I_O = 500 mA each			95	130	
				I_O = 500 mA each, T_J = 100°C			120	160	
		3.3V or 5V to xVPP, (see Note 1)		I_O = 50 mA each			0.8	1	Ω
				I_O = 50 mA each, T_J = 100°C			1	1.3	
		12V to xVPP, (see Note 1)		I_O = 50 mA each			2	2.5	
				I_O = 50 mA each, T_J = 100°C			2.5	3.4	
	Output discharge resistance	Discharge at xVCC		$I_{O(disc)}$ = 1 mA		0.5	0.7	1	kΩ
		Discharge at xVPP		$I_{O(disc)}$ = 1 mA		0.2	0.4	0.5	
I_{OS}	Short-circuit output current			Limit (steady-state value), output powered into a short circuit	$I_{OS(xVCC)}$	1	1.4	2	A
					$I_{OS(xVPP)}$	120	200	300	mA
				Limit (steady-state value), output powered into a short circuit, T_J = 100°C	$I_{OS(xVCC)}$	1	1.4	2	A
					$I_{OS(xVPP)}$	120	200	300	mA
	Thermal shutdown temperature (see Note 1)	Thermal trip point, T_J		Rising temperature			135		°C
		Hysteresis, T_J					10		
	Current-limit response time (see Note 2 and Note 3)			5V to xVCC = 5 V, with 100-mΩ short to GND			10		µs
				5V to xVPP = 5 V, with 100-mΩ short to GND			3		
I_I	Input current, quiescent	Normal operation	$I_{I(3.3V)}$	V_O(xVCC) = V_O(xVPP) = 3.3 V and also for $\overline{RESET}$ = 0 V			140	200	µA
			$I_{I(5V)}$				8	12	
			$I_{I(12V)}$				100	180	
		Shutdown mode	$I_{I(3.3V)}$	V_O(xVCC) = V_O(xVPP) = Hi-z			0.3	2	
			$I_{I(5V)}$				0.1	2	
			$I_{I(12V)}$				0.3	2	
I_{lkg}	Leakage current, output off state	Shutdown mode		$V_{O(xVCC)}$ = 5 V, $V_{I(5V)}$ = $V_{I(12V)}$ = 0 V				10	µA
					T_J = 100°C			50	
				$V_{O(xVPP)}$ = 12 V, $V_{I(5V)}$ = $V_{I(12V)}$ = 0 V				10	
					T_J = 100°C			50	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

NOTES: 1. SNP2x31, SNP2x41, SNP2x61: two switches on. SNP1x21: one switch on.
2. Specified by design; not tested in production.
3. From application of short to 110% of final current limit.

electrical characteristics, T_J = 25°C, $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V (not applicable for SNP2x31), all outputs unloaded (unless otherwise noted) (continued)

logic section (CLOCK, DATA, LATCH, $\overline{RESET}$, $\overline{SHDN}$, $\overline{OC}$)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current, logic	$I_{I(/RESET)}$ (see Note 3)	$\overline{RESET}$ = 5.5 V	−1		1	µA
			$\overline{RESET}$ = 0 V	−30	−20	−10	
		$I_{I(/SHDN)}$ (see Note 3)	$\overline{SHDN}$ = 5.5 V	−1		1	
			$\overline{SHDN}$ = 0 V	−50		−3	
		$I_{I(LATCH)}$ (see Note 3)	LATCH = 5.5 V			50	
			LATCH = 0 V	−1		1	
		$I_{I(CLOCK, DATA)}$	0 V to 5.5 V	−1		1	
V_{IH}	High-level input voltage, logic			2			V
V_{IL}	Low-level input voltage, logic					0.8	V
$V_{O(sat)}$	Output saturation voltage at $\overline{OC}$		I_O = 2 mA		0.14	0.4	V
I_{lkg}	Leakage current at $\overline{OC}$		$V_{O(/OC)}$ = 5.5 V		0	1	µA

NOTE 3: LATCH has low-current pulldown. $\overline{RESET}$ and $\overline{SHDN}$ have low-current pullup.

UVLO and POR (power-on reset)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(3.3V)}$	Input voltage at 3.3V pin, UVLO	3.3-V level below which all switches are Hi-Z	2.4	2.7	2.9	V
$V_{hys(3.3V)}$	UVLO hysteresis voltage at VA (see Note 1)			100		mV
$V_{I(5V)}$	Input voltage at 5V pin, UVLO	5-V level below which only 5V switches are Hi-Z	2.3	2.5	2.9	V
$V_{hys(5V)}$	UVLO hysteresis voltage at 5V (see Note 1)			100		mV
t_{df}	Delay time for falling response, UVLO (see Note 1)	Delay from voltage hit (step from 3 V to 2.3 V) to Hi-Z control (90% V_G to GND)		4		µs
$V_{I(POR)}$	Input voltage, power-on reset (see Note 1)	3.3-V voltage below which POR is asserted causing a RESET internally with all line switches open and all discharge switches closed.			1.7	V

NOTE 1: Specified by design; not tested in production.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, $V_{I(3.3V)}$ = 3.3 V, $V_{I(5V)}$ = 5 V, $V_{I(12)}$ = 12 V (not applicable for SNP2x31) all outputs unloaded (unless otherwise noted)

PARAMETER†		LOAD CONDITION	TEST CONDITIONS‡		MIN	TYP	MAX	UNIT
t_r	Output rise times (see Note 1)	$C_{L(xVCC)}$= 0.1 µF, $C_{L(xVPP)}$= 0.1 µF, $I_{O(xVCC)}$ = 0 A, $I_{O(xVPP)}$ = 0 A	$V_{O(xVCC)}$ = 5 V			0.9		ms
			$V_{O(xVPP)}$ = 12 V			0.26		
		$C_{L(xVCC)}$= 150 µF, $C_{L(xVPP)}$= 10 µF, $I_{O(xVCC)}$ = 0.75 A, $I_{O(xVPP)}$ = 50 mA	$V_{O(xVCC)}$ = 5 V			1.1		
			$V_{O(xVPP)}$ = 12 V			0.6		
t_f	Output fall times (see Note 1)	$C_{L(xVCC)}$= 0.1 µF, $C_{L(xVPP)}$= 0.1 µF, $I_{O(xVCC)}$ = 0 A, $I_{O(xVPP)}$ = 0 A	$V_{O(xVCC)}$ = 5 V, Discharge switches ON			0.5		ms
			$V_{O(xVPP)}$ = 12 V, Discharge switches ON			0.2		
		$C_{L(xVCC)}$= 150 µF, $C_{L(xVPP)}$= 10 µF, $I_{O(xVCC)}$ = 0.75 A, $I_{O(xVPP)}$ = 50 mA	$V_{O(xVCC)}$ = 5 V			2.35		
			$V_{O(xVPP)}$ = 12 V			3.9		
t_{pd}	Propagation delay times (see Note 1)	$C_{L(xVCC)}$= 0.1 µF, $C_{L(xVPP)}$= 0.1 µF, $I_{O(xVCC)}$ = 0 A, $I_{O(xVPP)}$ = 0 A	Latch↑ to xVPP (12 V)§	t_{pdon}		2		ms
				t_{pdoff}		0.62		
			Latch↑ to xVPP (5 V)	t_{pdon}		0.77		
				t_{pdoff}		0.51		
			Latch↑ to xVPP (3.3 V)	t_{pdon}		0.75		
				t_{pdoff}		0.52		
			Latch↑ to xVCC (5 V)	t_{pdon}		0.3		
				t_{pdoff}		2.5		
			Latch↑ to xVCC (3.3V)	t_{pdon}		0.3		
				t_{pdoff}		2.8		
		$C_{L(xVCC)}$= 150 µF, $C_{L(xVPP)}$= 10 µF, $I_{O(xVCC)}$ = 0.75 A, $I_{O(xVPP)}$ = 50 mA	Latch↑ to xVPP (12 V)§	t_{pdon}		2.2		ms
				t_{pdoff}		0.8		
			Latch↑ to xVPP (5 V)	t_{pdon}		0.8		
				t_{pdoff}		0.6		
			Latch↑ to xVPP (3.3 V)	t_{pdon}		0.8		
				t_{pdoff}		0.6		
			Latch↑ to xVCC (5 V)	t_{pdon}		0.6		
				t_{pdoff}		2.5		
			Latch↑ to xVCC (3.3V)	t_{pdon}		0.5		
				t_{pdoff}		2.6		

† Refer to Parameter Measurement Information in Figure 1.
‡ No card inserted, assumes a 0.1-µF output capacitor (see Figure 1).
§ Not applicable for SNP2x31
NOTE 1: Specified by design; not tested in production.

PARAMETER MEASUREMENT INFORMATION

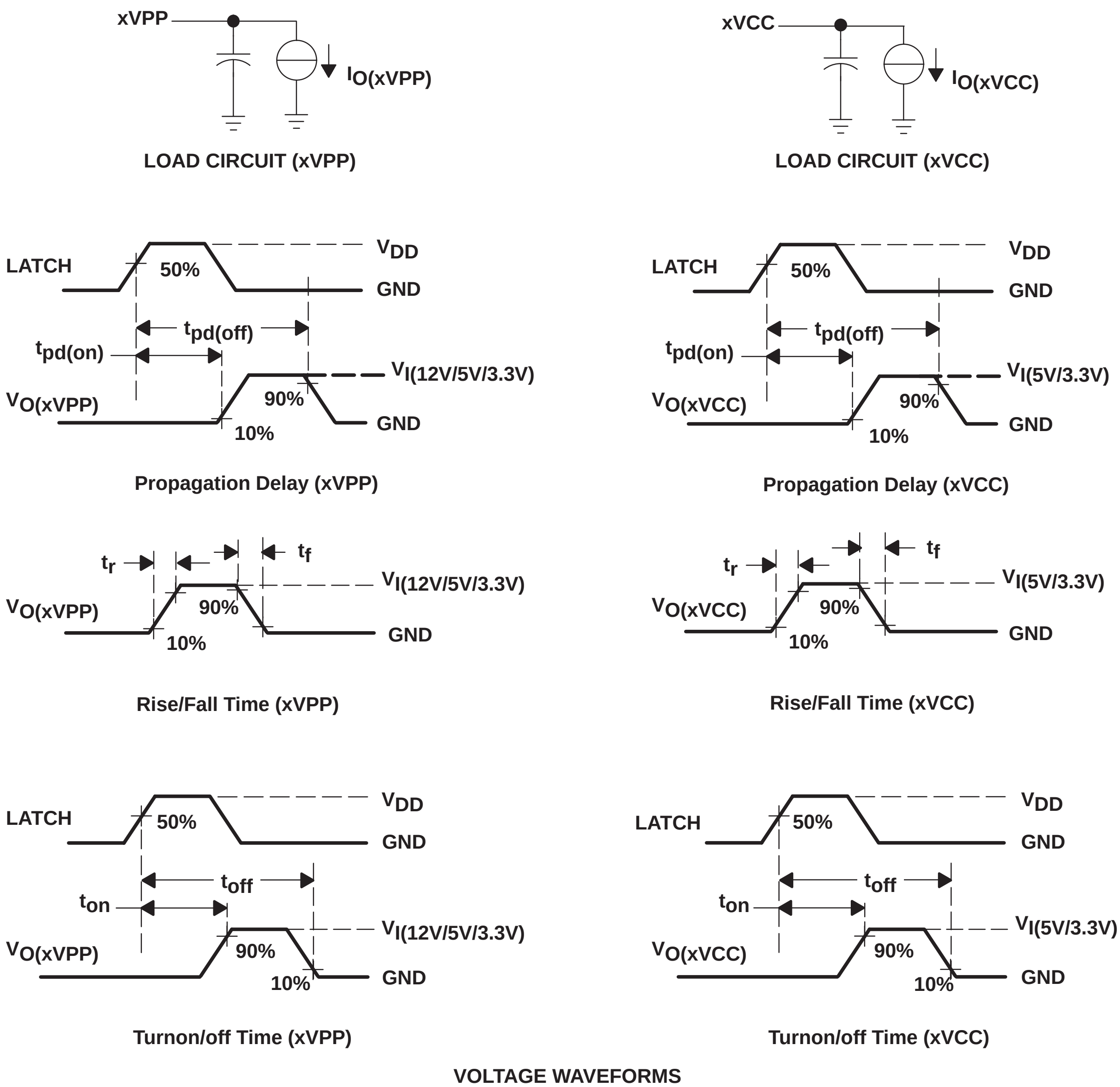
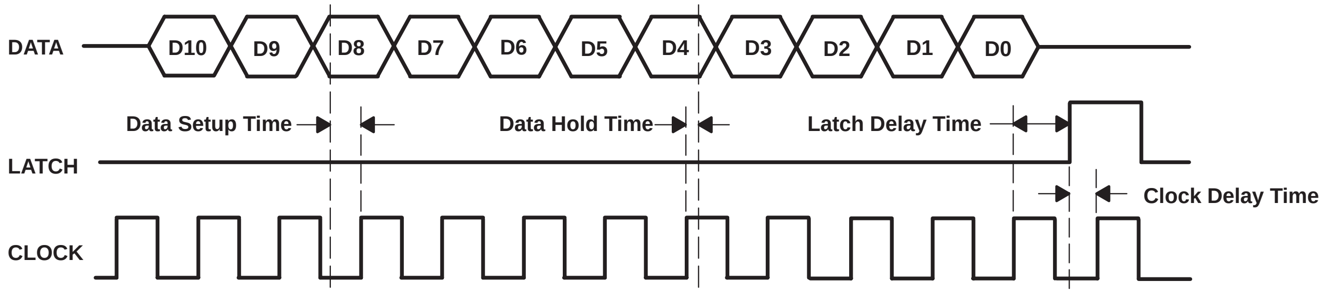


Figure 1. Test Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: Data is clocked in on the positive edge of the clock. The positive edge of the latch signal should occur before the next positive edge of the clock. For definition of D0 to D10, see the control logic table.

Figure 2. Serial-Interface Timing for SNP2x61

Table of Graphs

		FIGURE
Short-circuit response, short applied to powered-on 5-V xVCC-switch output	vs Time	3
Short-circuit response, short applied to powered-on 12-V xVPP-switch output	vs Time	4
$\overline{OC}$ response with ramped overcurrent-limit load on 5-V xVCC-switch output	vs Time	5
$\overline{OC}$ response with ramped overcurrent-limit load on 12-V xVPP-switch output	vs Time	6
xVCC Turnon propagation delay time (C_L = 150 µF)	vs Junction temperature	7
xVCC Turnoff propagation delay time (C_L = 150 µF)	vs Junction temperature	8
xVPP Turnon propagation delay time (C_L = 10 µF)	vs Junction temperature	9
xVPP Turnoff propagation delay time (C_L = 10 µF)	vs Junction temperature	10
xVCC Turnon propagation delay time (T_J = 25°C)	vs Load capacitance	11
xVCC Turnoff propagation delay time (T_J = 25°C)	vs Load capacitance	12
xVPP Turnon propagation delay time (T_J = 25°C)	vs Load capacitance	13
xVPP Turnoff propagation delay time (T_J = 25°C)	vs Load capacitance	14
xVCC Rise time (C_L = 150 µF)	vs Junction temperature	15
xVCC Fall time (C_L = 150 µF)	vs Junction temperature	16
xVPP Rise time (C_L = 10 µF)	vs Junction temperature	17
xVPP Fall time (C_L = 10 µF)	vs Junction temperature	18
xVCC Rise time (T_J = 25°C)	vs Load capacitance	19
xVCC Fall time (T_J = 25°C)	vs Load capacitance	20
xVPP Rise time (T_J = 25°C)	vs Load capacitance	21
xVPP Fall time (T_J = 25°C)	vs Load capacitance	22

PARAMETER MEASUREMENT INFORMATION

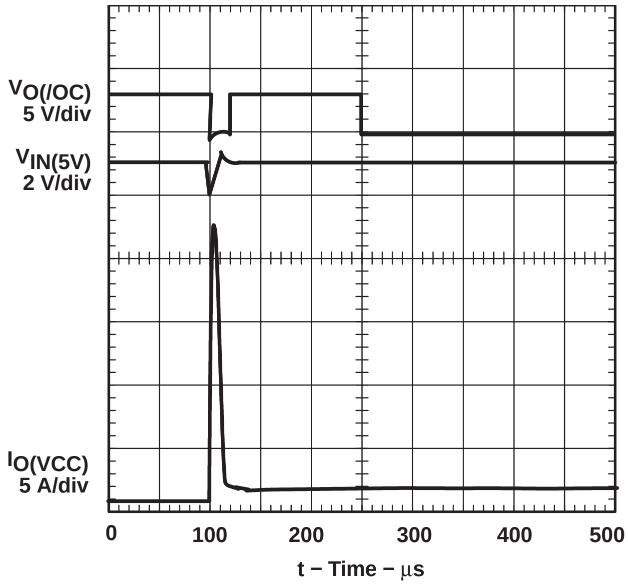


Figure 3. Short-Circuit Response, Short Applied to Powered-on 5-V xVCC-Switch Output

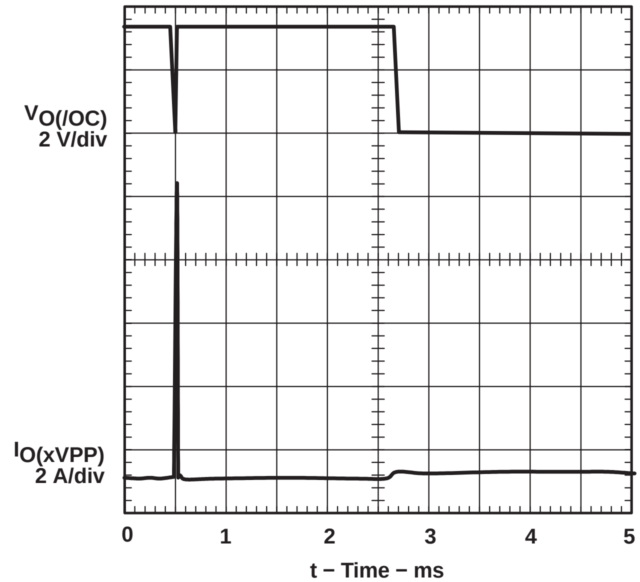


Figure 4. Short-Circuit Response, Short Applied to Powered-on 12-V xVPP-Switch Output

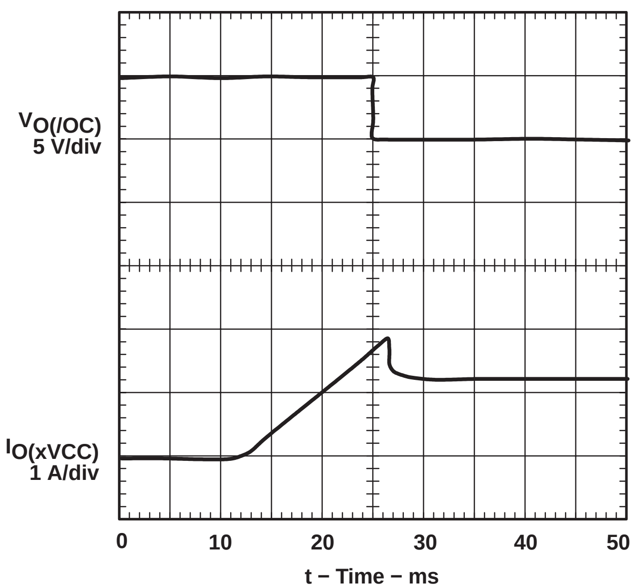


Figure 5. $\overline{OC}$ Response With Ramped Overcurrent-Limit Load on 5-V xVCC-Switch Output

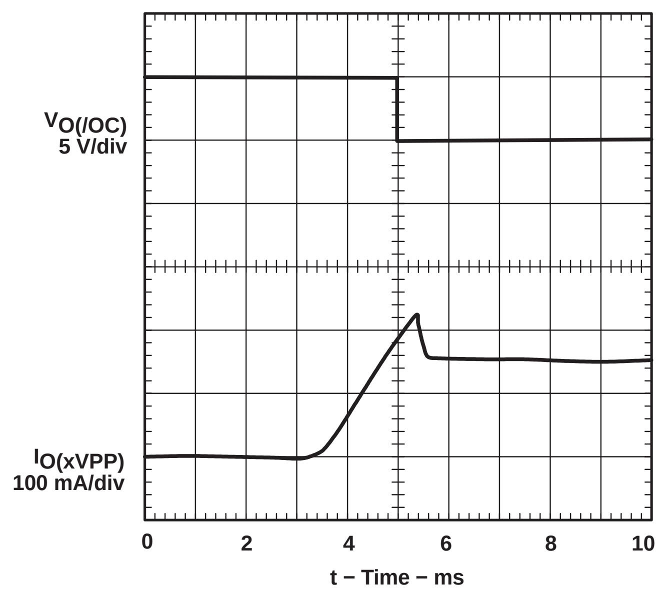


Figure 6. $\overline{OC}$ Response With Ramped Overcurrent-Limit Load on 12-V xVPP-Switch Output

PARAMETER MEASUREMENT INFORMATION

TURNON PROPAGATION DELAY TIME, xVCC vs JUNCTION TEMPERATURE

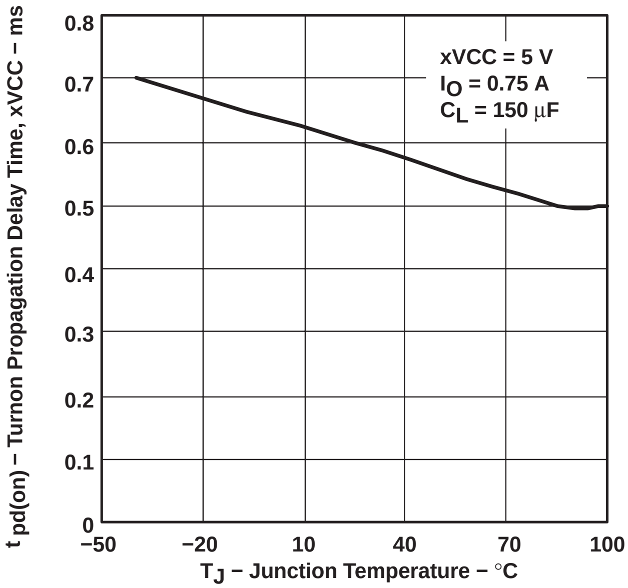


Figure 7

TURNOFF PROPAGATION DELAY TIME, xVCC vs JUNCTION TEMPERATURE

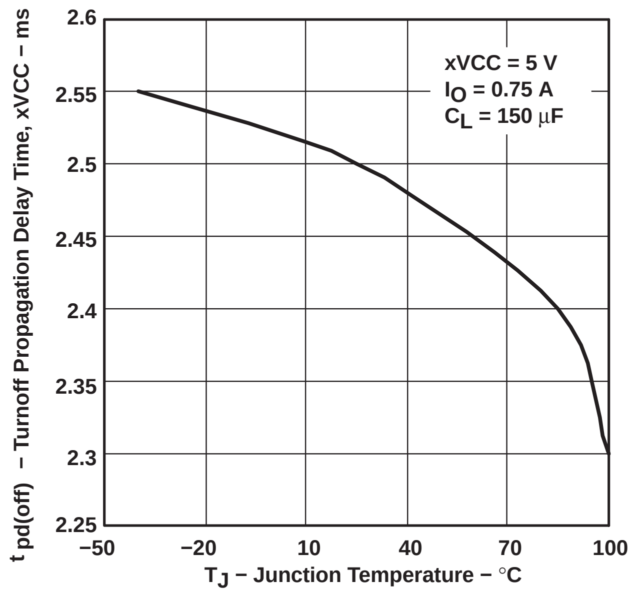


Figure 8

TURNON PROPAGATION DELAY TIME, xVPP vs JUNCTION TEMPERATURE

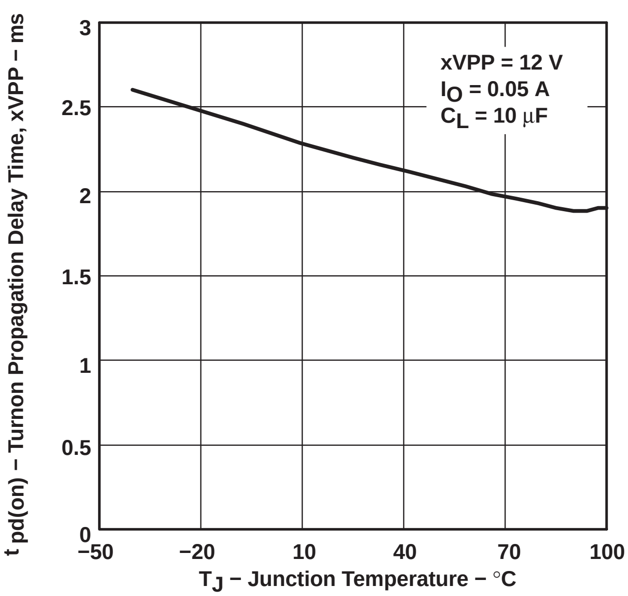


Figure 9

TURNOFF PROPAGATION DELAY TIME, xVPP vs JUNCTION TEMPERATURE

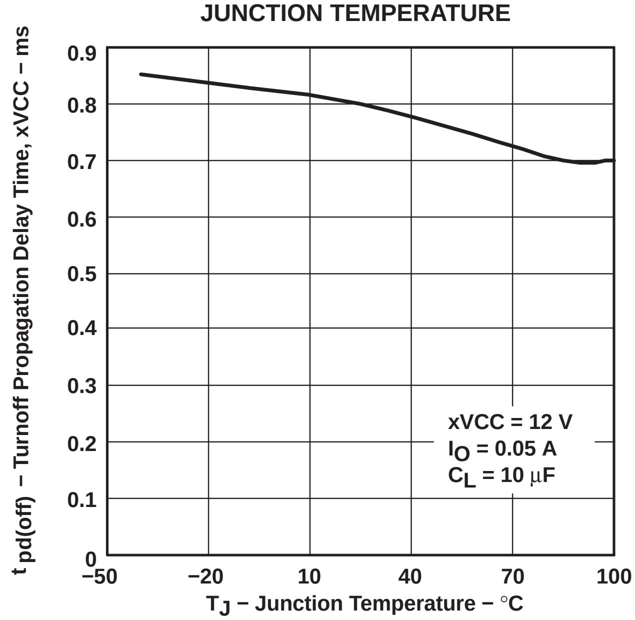


Figure 10

PARAMETER MEASUREMENT INFORMATION

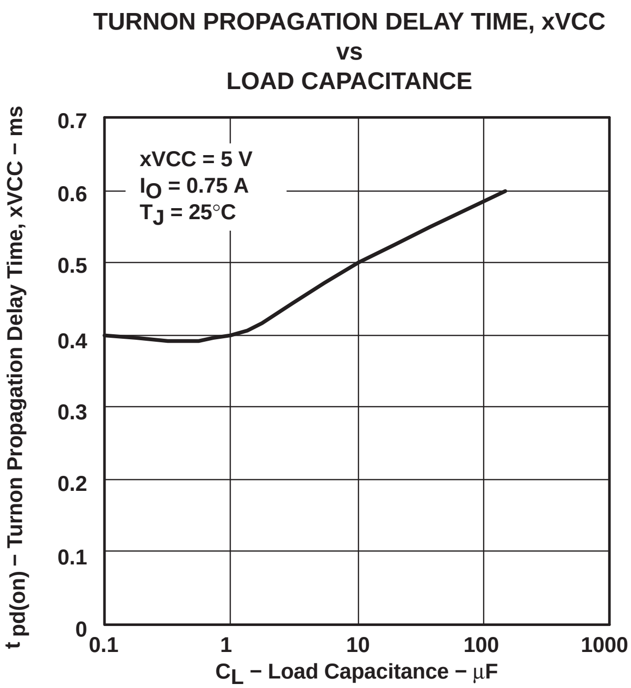


Figure 11

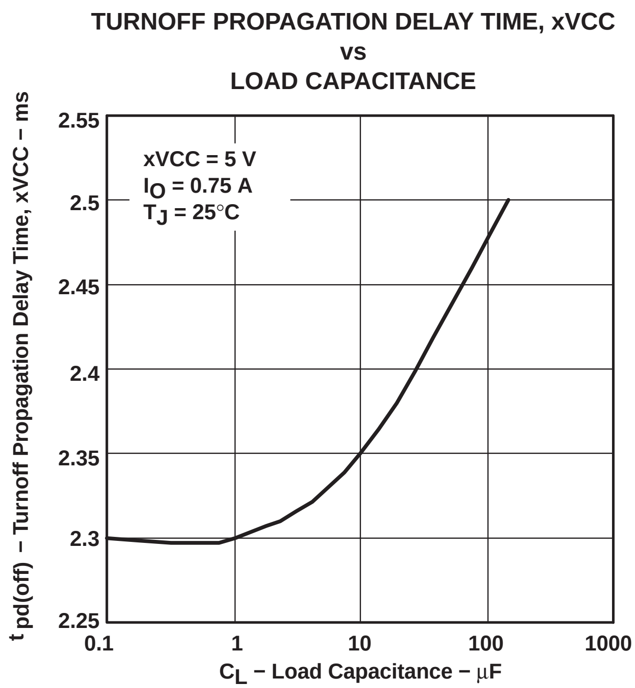


Figure 12

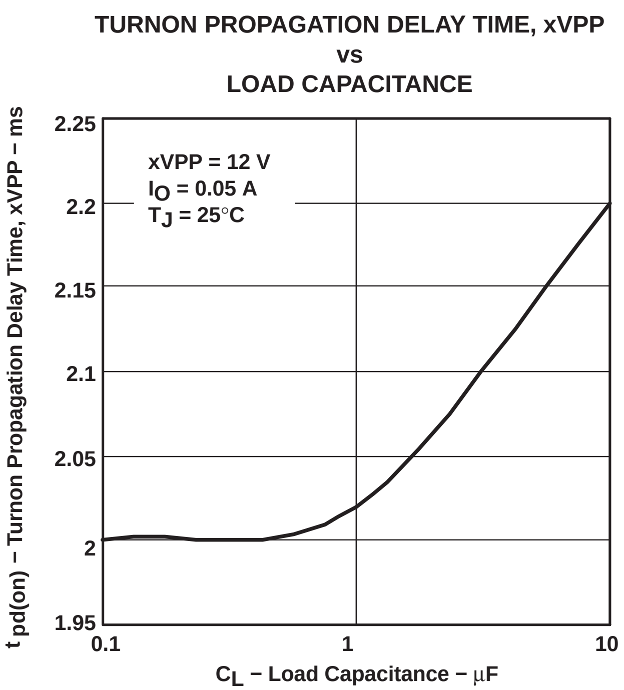


Figure 13

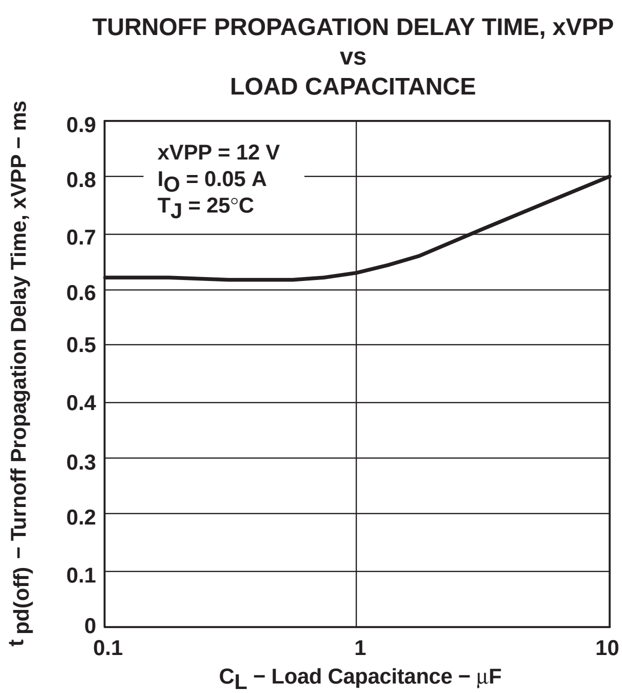


Figure 14

PARAMETER MEASUREMENT INFORMATION

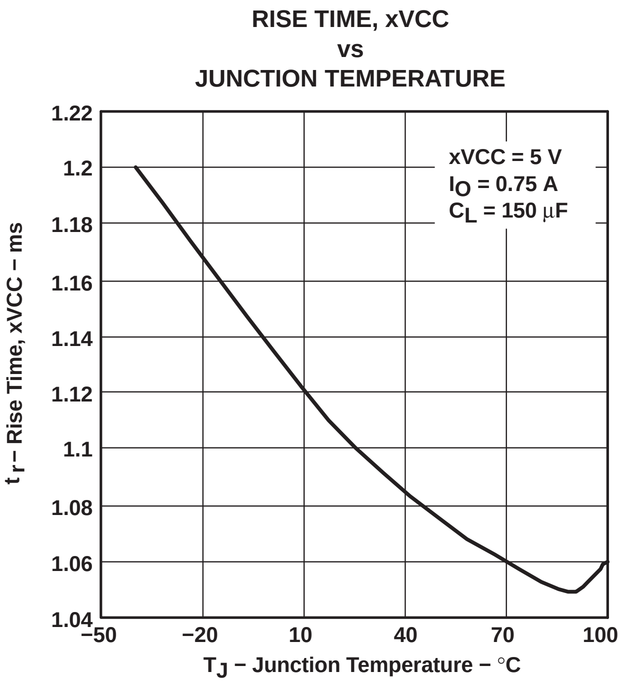


Figure 15

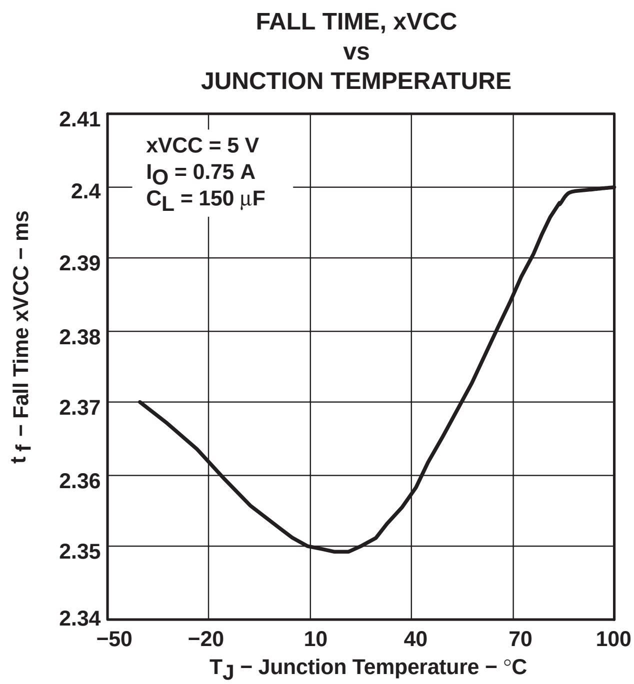


Figure 16

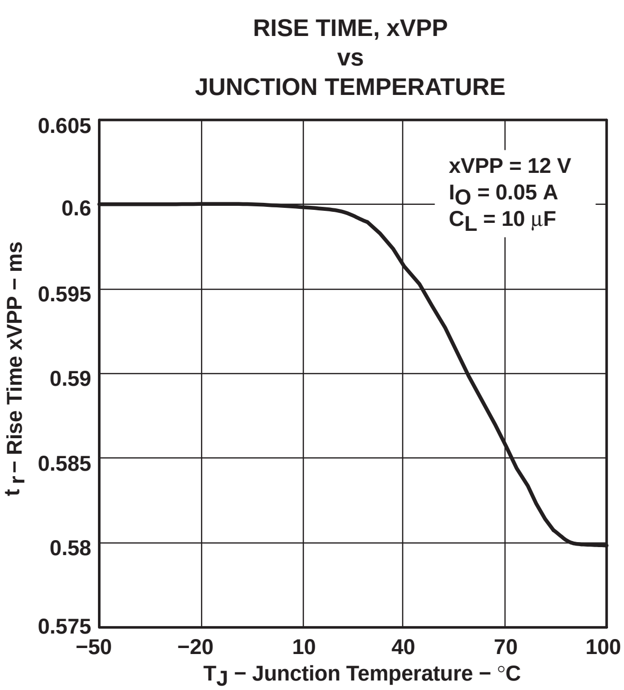


Figure 17

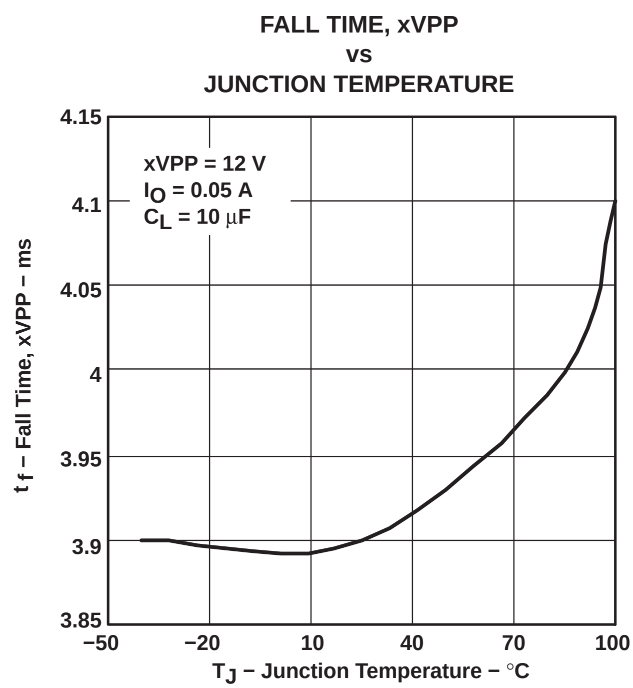


Figure 18

PARAMETER MEASUREMENT INFORMATION

**RISE TIME, xVCC
vs
LOAD CAPACITANCE**

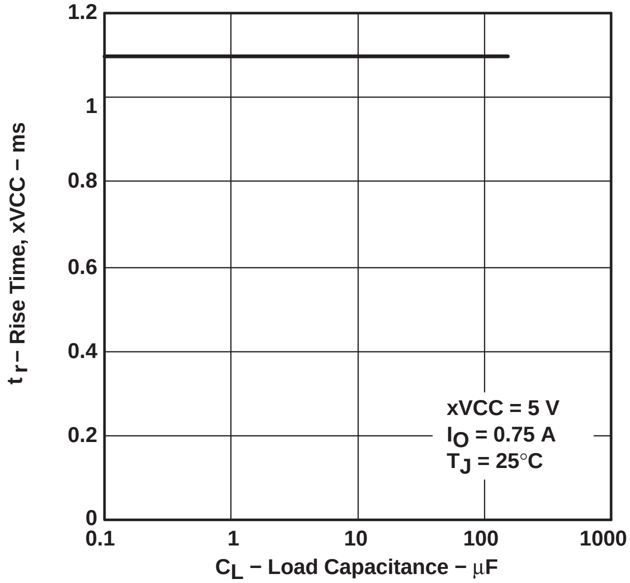


Figure 19

**FALL TIME, xVCC
vs
LOAD CAPACITANCE**

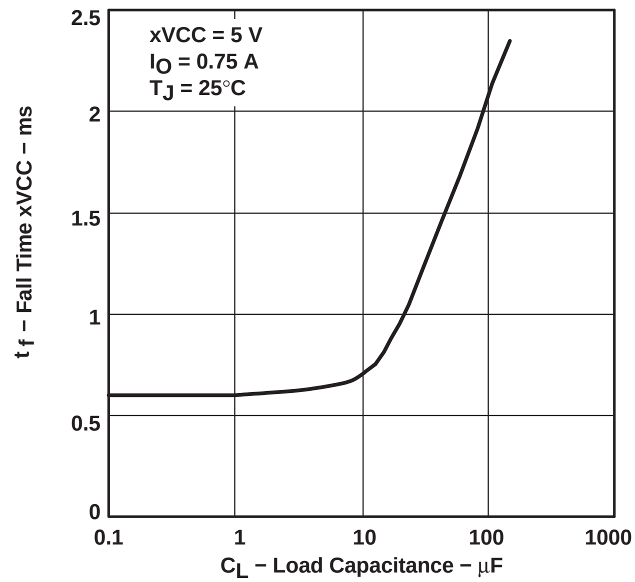


Figure 20

**RISE TIME, xVPP
vs
LOAD CAPACITANCE**

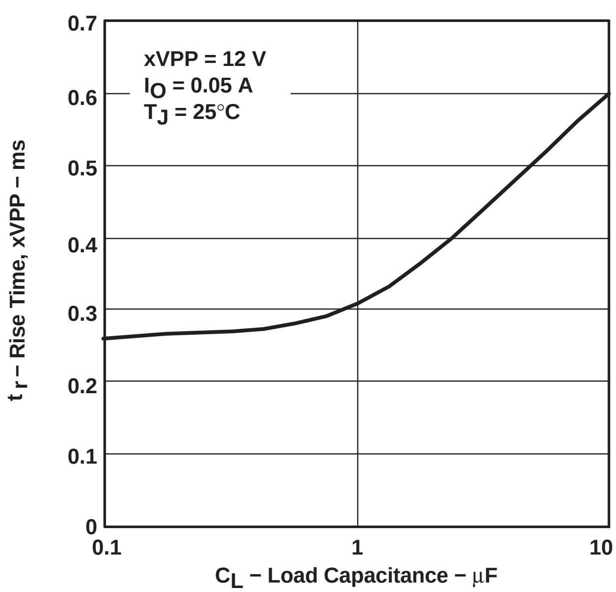


Figure 21

**FALL TIME, xVPP
vs
LOAD CAPACITANCE**

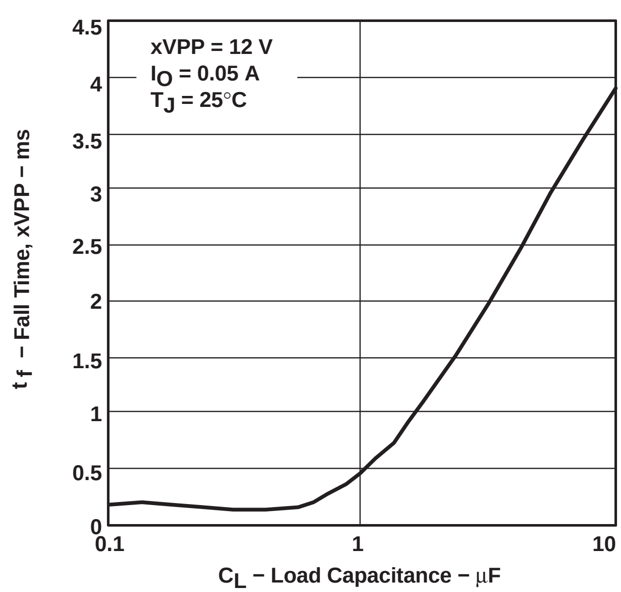


Figure 22

TYPICAL CHARACTERISTICS

Table of Graphs

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INPUT CURRENT, xVCC = 3.3 V vs JUNCTION TEMPERATURE

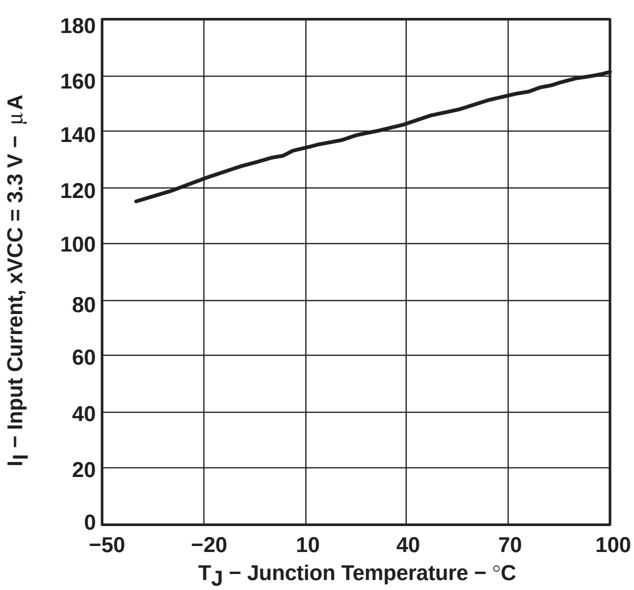


Figure 23

INPUT CURRENT, xVCC = 5 V vs JUNCTION TEMPERATURE

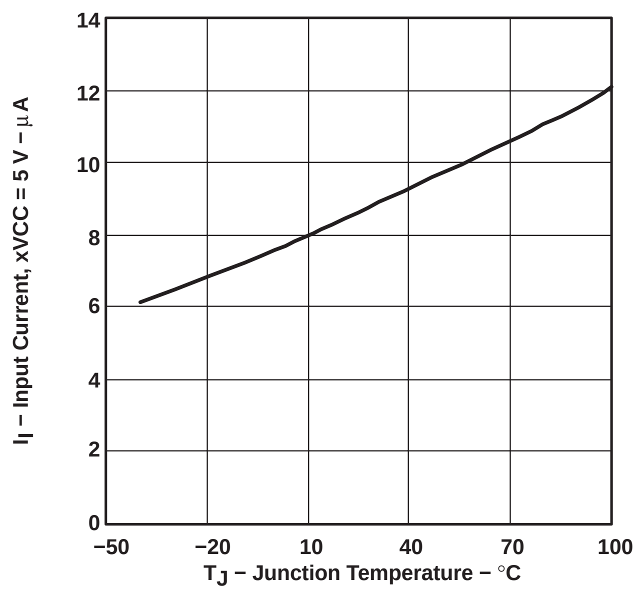


Figure 24

TYPICAL CHARACTERISTICS

INPUT CURRENT, xVPP = 12 V
vs
JUNCTION TEMPERATURE

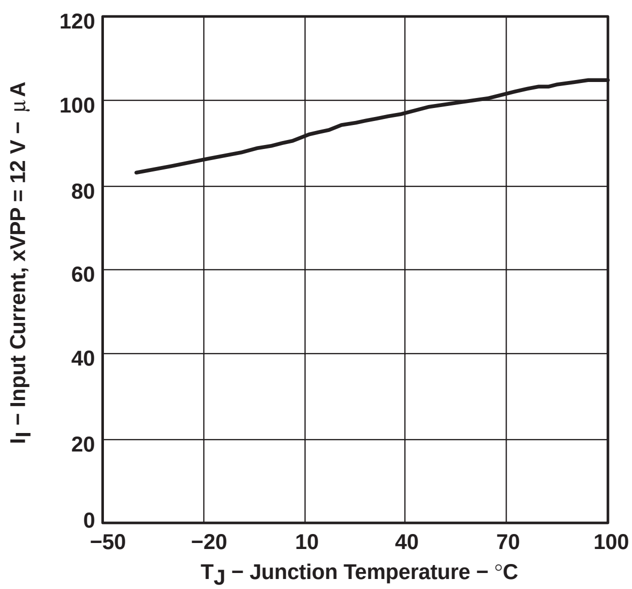


Figure 25

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
3.3 V TO xVCC SWITCH
vs
JUNCTION TEMPERATURE

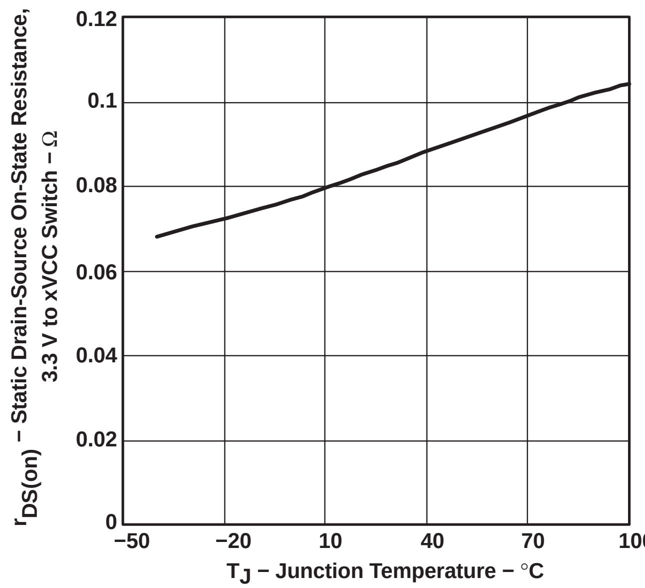


Figure 26

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
5 V TO xVCC SWITCH
vs
JUNCTION TEMPERATURE

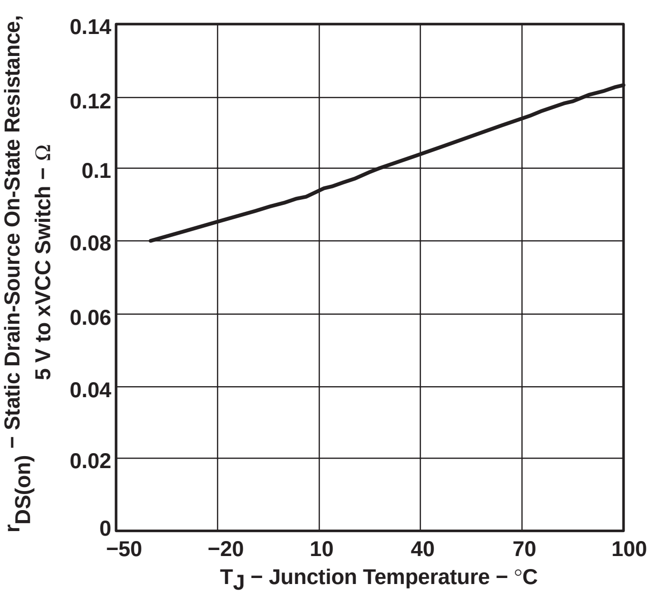


Figure 27

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
12 V TO xVPP SWITCH
vs
JUNCTION TEMPERATURE

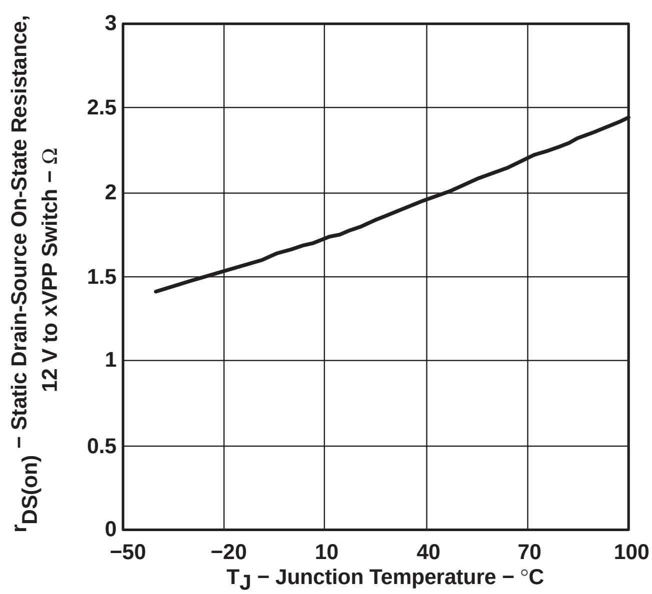


Figure 28

TYPICAL CHARACTERISTICS

xVCC SWITCH VOLTAGE DROP, 3.3-V INPUT vs LOAD CURRENT

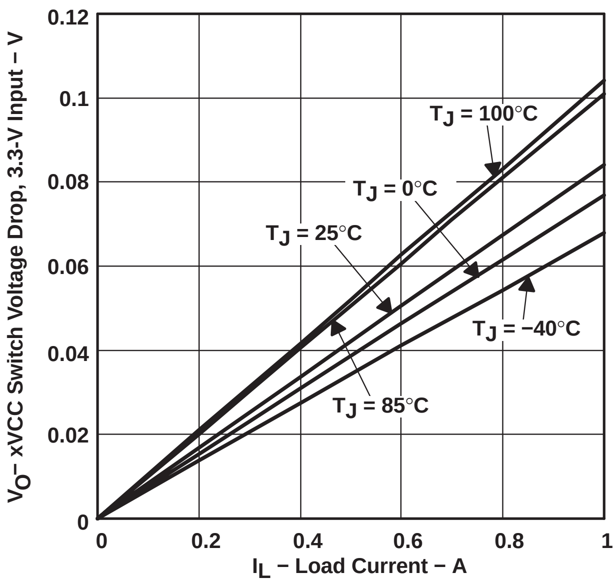


Figure 29

xVCC SWITCH VOLTAGE DROP, 5-V INPUT vs LOAD CURRENT

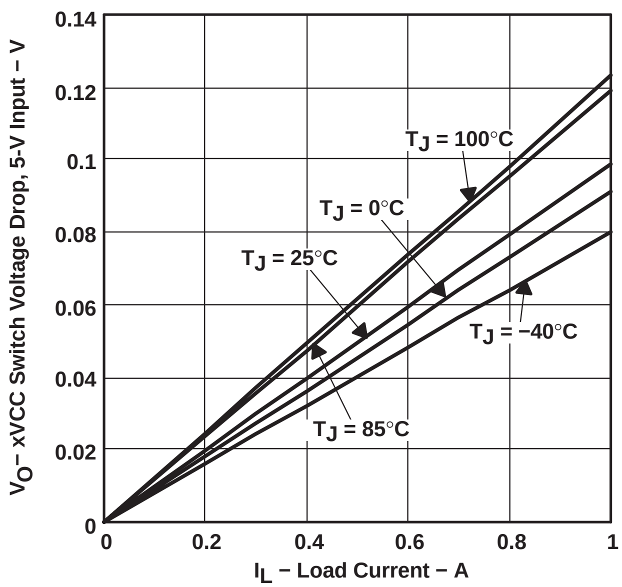


Figure 30

xVPP SWITCH VOLTAGE DROP, 12-V INPUT vs LOAD CURRENT

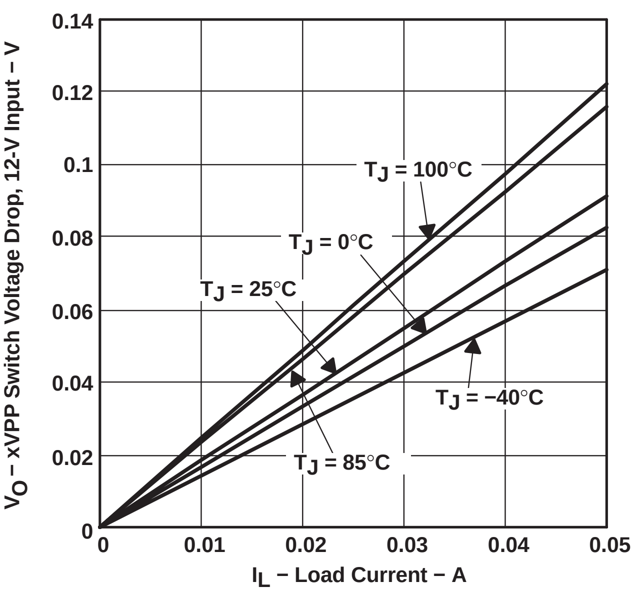


Figure 31

SHORT-CIRCUIT CURRENT LIMIT, 3.3 V TO xVCC vs JUNCTION TEMPERATURE

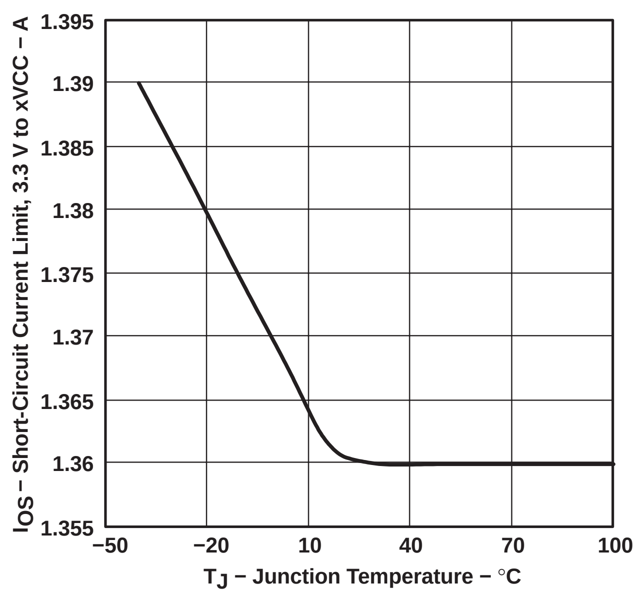


Figure 32

TYPICAL CHARACTERISTICS

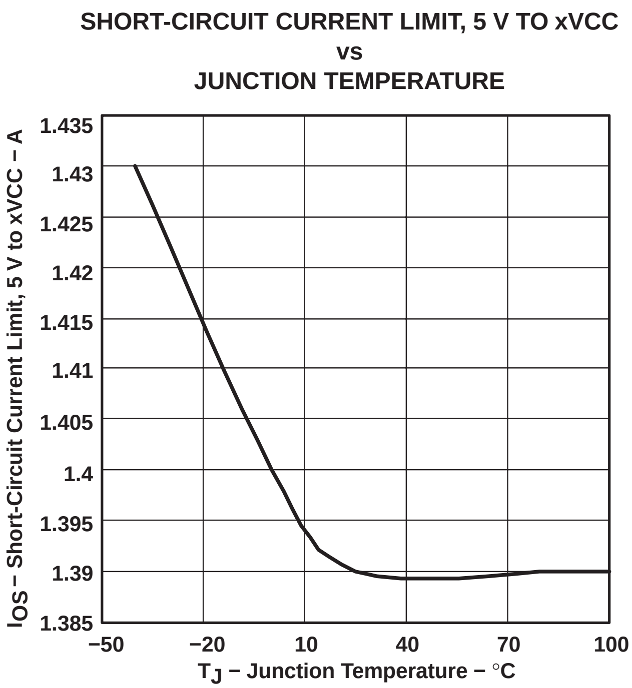


Figure 33

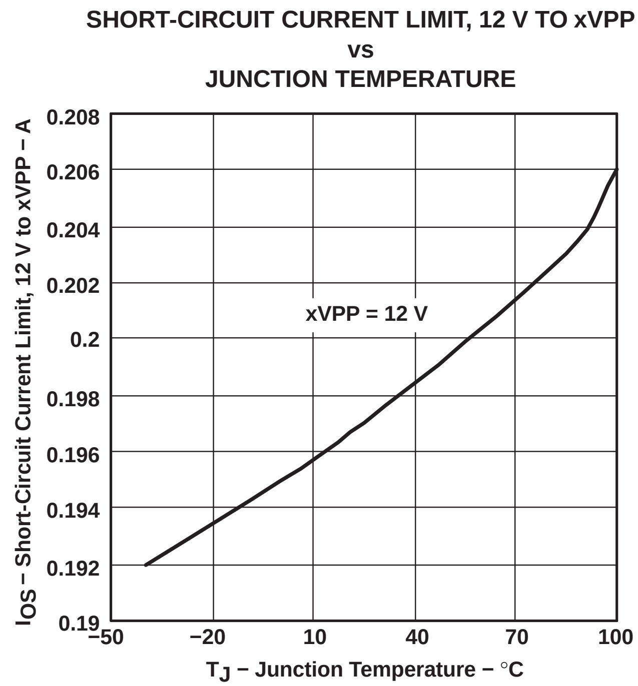


Figure 34

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add flash memory to portable computers. The idea of add-in cards quickly took hold, and modems, wireless LANs, global positioning satellite system (GPS), multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established, comprising members from leading computer, software, PC Card, and semiconductor manufacturers. One key goal was to realize the *plug-and-play* concept, so that cards and hosts from different vendors would be transparently compatible.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connector. This power interface consists of two V_{CC}, two V_{pp}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals, but are normally tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{pp} terminals. Cardbus cards of today typically do not use 12 V, which is now more of an optional requirement in the host.

designing for voltage regulation

The current PCMCIA specification for output voltage regulation, $V_{O(reg)}$, of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply has an output-voltage regulation, $V_{PS(reg)}$, of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card results from resistive losses, V_{PCB}, in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop, V_{DS}, for the SNP1x21, SNP2x31, SNP2x41, and SNP2x61 would be the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB}$$

Typically, this would leave 100 mV for the allowable voltage drop across the 5-V switch. The specification for output voltage regulation of the 3.3-V output is 300 mV; therefore, using the same equation by deducting the voltage drop percentages (2%) for power-supply regulation and PCB resistive loss (1%), the allowable voltage drop for the 3.3-V switch is 200 mV. The voltage drop is the output current multiplied by the switch resistance of the device. Therefore, the maximum output current, I_O max, that can be delivered to the PC Card in regulation is the allowable voltage drop across the IC, divided by the output-switch resistance.

$$I_O max = \frac{V_{DS}}{r_{DS(on)}}$$

The xVCC outputs have been designed to deliver the peak and average currents defined by the PC Card specification within regulation over the operating temperature range. The xVPP outputs of the device have been designed to deliver 100 mA continuously.

APPLICATION INFORMATION

overcurrent and overtemperature protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power-supply or PCB trace damage. Even extremely robust systems could undergo rapid battery discharge into a damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. The reliability of fused systems is poor, in comparison, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The SNP1x21, SNP2x31, SNP2x41, and SNP2x61 take a two-pronged approach to overcurrent protection, which is designed to activate if an output is shorted or when an overcurrent condition is present when switches are powered up. First, instead of fuses, sense FETs monitor each of the xVCC and xVPP power outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. Excessive current generates an error signal that limits the output current of only the affected output, preventing damage to the host. Each xVCC output overcurrent limits from 1 A to 2.2 A, typically around 1.6 A; the xVPP outputs limit from 100 mA to 250 mA, typically around 200 mA.

Second, when an overcurrent condition is detected, the SNP1x21, SNP2x31, SNP2x41, and SNP2x61 assert an active low $\overline{OC}$ signal that can be monitored by the microprocessor or controller to initiate diagnostics and/or send the user a warning message. If an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates, shutting down all power outputs until the device cools to within a safe operating region, which is ensured by a thermal shutdown hysteresis. Thermal limiting prevents destruction of the IC from overheating beyond the package power-dissipation ratings.

During power up, the devices control the rise times of the xVCC and xVPP outputs and limit the inrush current into a large load capacitance, faulty card, or connector.

12-V supply not required

Some PC Card switches use the externally supplied 12 V to power gate drive and other chip functions, which requires that power be present at all times. The SNP1x21, SNP2x41 and SNP2x61 offer considerable power savings by using an internal charge pump to generate the required higher gate drive voltages from the 3.3-V input. Therefore, the external 12-V supply can be disabled except when needed by the PC Card in the slot, thereby extending battery lifetime. A special feature in the 12-V circuitry actually helps to reduce the supply current demanded from the 3.3-V input. When 12 V is supplied and requested at the VPP output, a voltage selection circuit will draw the charge-pump drive current for the 12-V FETs from the 12-V input. This selection is automatic and effectively reduces demand fluctuations on the normal 3.3-V VCC rail. For proper operation of this feature, a minimum 3.3-V input capacitance of 4.7 µF is recommended, and a minimum 12-V input ramp-up rate of 12 V/50 ms (240 V/s) is required. Additional power savings are realized during a software shutdown in which quiescent current drops to a maximum of 1 µA.

voltage-transitioning requirement

PC Cards, like portables, are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The SNP1x21, SNP2x31, SNP2x41, and SNP2x61 meet all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This action ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. PC Card specification requires that V_{CC} be discharged within 100 ms. PC Card resistance cannot be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. The devices include discharge transistors on all xVCC and xVPP outputs to meet the specification requirement.

APPLICATION INFORMATION

shutdown mode

In the shutdown mode, which can be controlled by $\overline{\text{SHDN}}$ or bit D8 of the input serial DATA word, each of the xVCC and xVPP outputs is forced to a high-impedance state. In this mode, the chip quiescent current is reduced to 1 µA or less to conserve battery power.

power-supply considerations

These switches have multiple pins for each 3.3-V (except for SNP1x21) and 5-V power input and for the switched xVCC outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is higher than that specified, resulting in increased voltage drops and power loss. It is recommended that all input and output power pins be paralleled for optimum operation.

To increase the noise immunity of the SNP1x21, SNP2x31, SNP2x41, and SNP2x61, the power-supply inputs should be bypassed with at least a 4.7-µF electrolytic or tantalum capacitor paralleled by a 0.047-µF to 0.1-µF ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1-µF (or larger) ceramic capacitor; doing so improves the immunity of the IC to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the devices and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken below −0.3 V.

$\overline{\text{RESET}}$ input

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying low-impedance paths from xVCC and xVPP terminals to ground. A low-impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The active low $\overline{\text{RESET}}$ input closes internal ground switches S1, S4, S7, and S11 with all other switches left open. The SNP1x21, SNP2x31, SNP2x41, and SNP2x61 remain in the low-impedance output state until the signal is deasserted and further data is clocked in and latched. The input serial data cannot be latched during reset mode. $\overline{\text{RESET}}$ is provided for direct compatibility with systems that use an active-low reset voltage supervisor. The $\overline{\text{RESET}}$ pin has an internal 150-kΩ pullup resistor.

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 26 through 28, using an initial temperature estimate about 30°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

Next, sum the power dissipation of all switches and calculate the junction temperature:

$$T_J = \left(\sum P_D \times R_{\theta JA}\right) + T_A$$

where:

$R_{\theta JA}$ is the inverse of the derating factor given in the dissipation rating table.

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

APPLICATION INFORMATION

logic inputs and outputs

The serial interface consists of the DATA, CLOCK, and LATCH leads. The data is clocked in on the positive edge of the clock (see Figure 2). The 11-bit (D0−D10) serial data word is loaded during the positive edge of the latch signal. The positive edge of the latch signal should occur before the next positive edge of the clock occurs.

The serial interface of the device is compatible with serial-interface PCMCIA controllers.

An overcurrent output ($\overline{\text{OC}}$) is provided to indicate an overcurrent or overtemperature condition in any of the xVCC and xVPP outputs as previously discussed.

SNP1x21, SNP2x31, SNP2x41, and SNP2x61 control logic

xVPP

	AVPP CONTROL SIGNALS			OUTPUT V_AVPP	BVPP CONTROL SIGNALS				OUTPUT V_BVPP
D8 ($\overline{\text{SHDN}}$)	D0	D1	D9		D8 ($\overline{\text{SHDN}}$)	D4	D5	D10	
1	0	0	X	0 V	1	0	0	X	0 V
1	0	1	0	3.3 V	1	0	1	0	3.3 V
1	0	1	1	5 V	1	0	1	1	5 V
1	1	0	X	12 V†	1	1	0	X	12 V†
1	1	1	X	Hi-Z	1	1	1	X	Hi-Z
0	X	X	X	Hi-Z	0	X	X	X	Hi-Z

† The output V_xVPP is Hi-Z for SNP2x31.

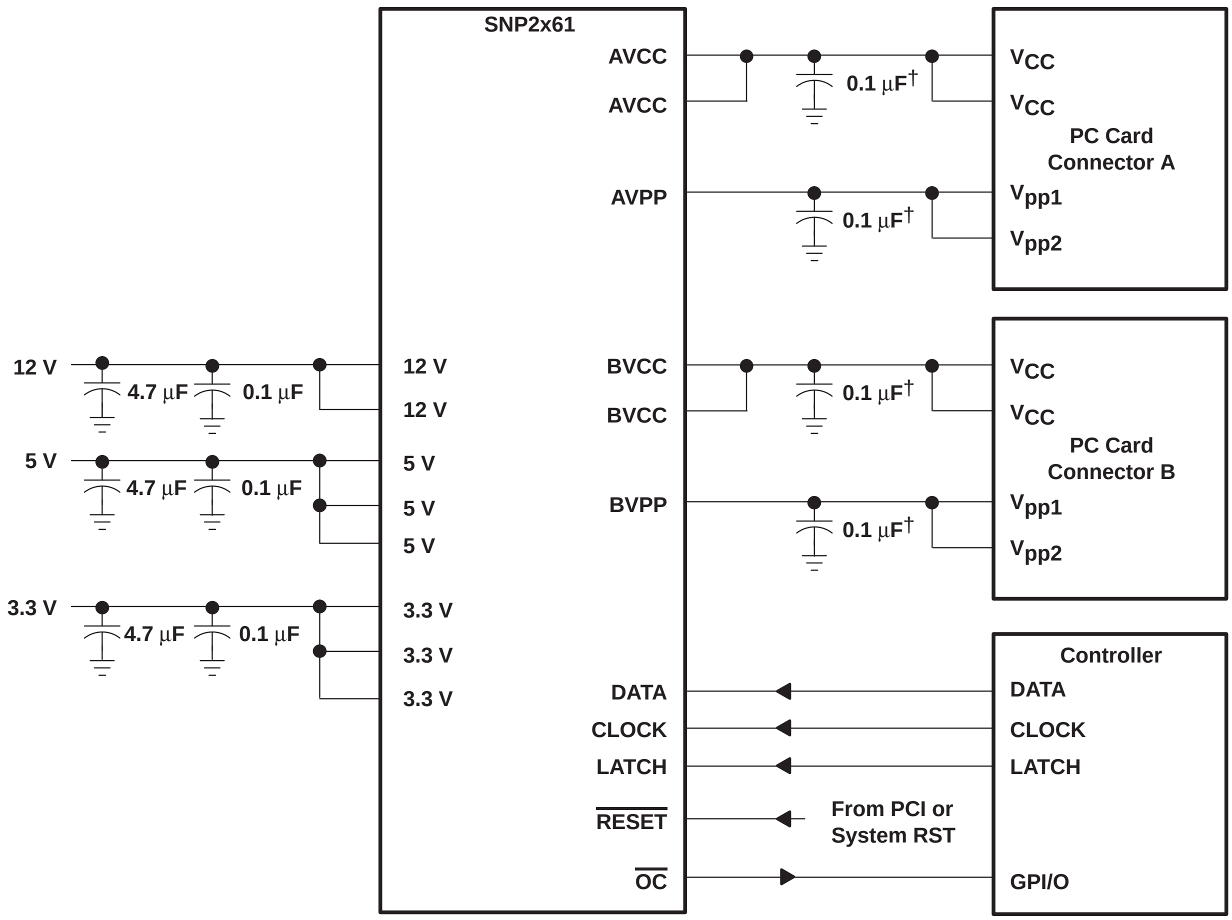
xVCC

	AVCC CONTROL SIGNALS		OUTPUT V_AVCC	BVCC CONTROL SIGNALS			OUTPUT V_BVCC
D8 ($\overline{\text{SHDN}}$)	D3	D2		D8 ($\overline{\text{SHDN}}$)	D6	D7	
1	0	0	0 V	1	0	0	0 V
1	0	1	3.3 V	1	0	1	3.3 V
1	1	0	5 V	1	1	0	5 V
1	1	1	0 V	1	1	1	0 V
0	X	X	Hi-Z	0	X	X	Hi-Z

APPLICATION INFORMATION

ESD protections (see Figure 35)

All inputs and outputs of these devices incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The xVCC and xVPP outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.



† Maximum recommended output capacitance for xVCC is 220 µF including card capacitance, and for xVPP is 10 µF, without OC glitch when switches are powered on.

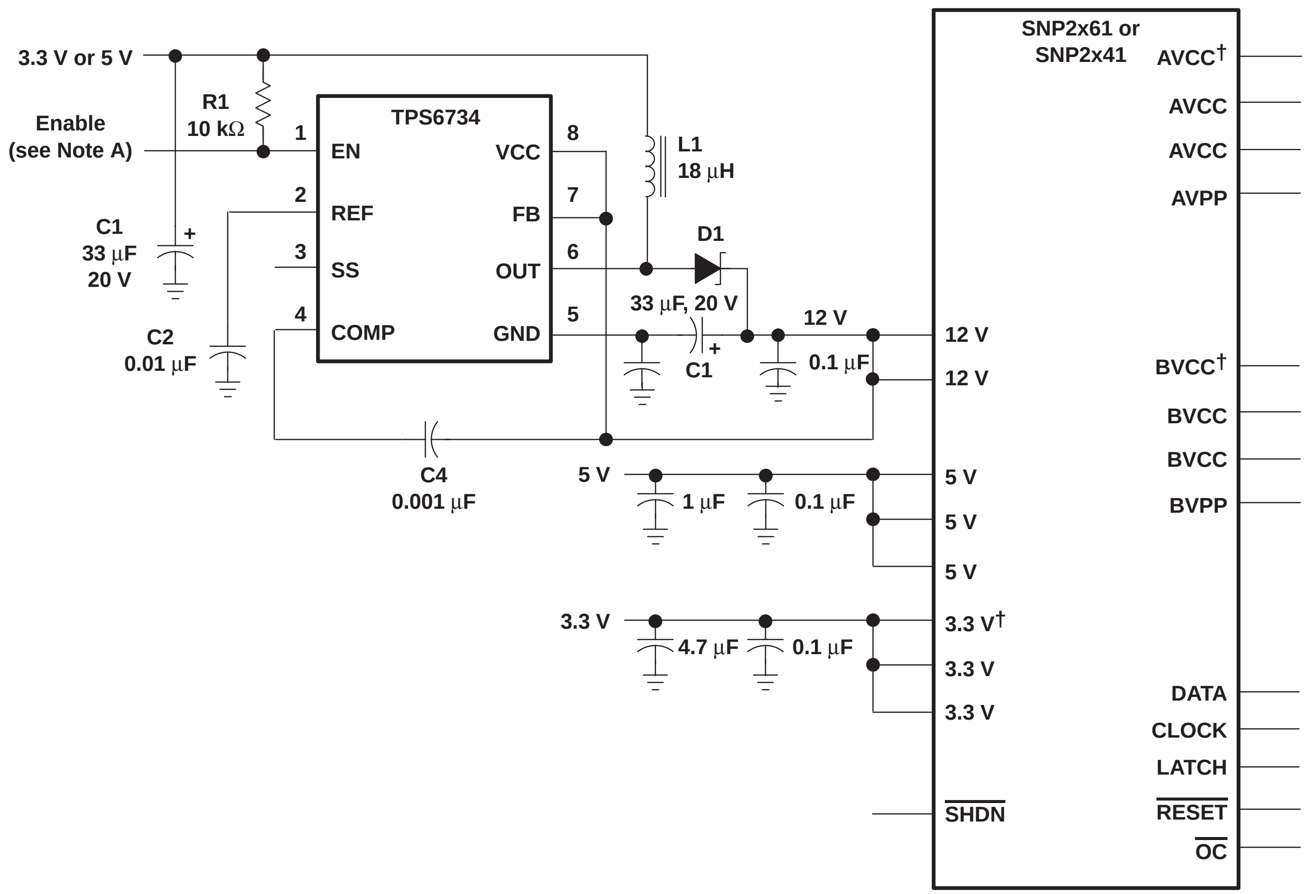
Figure 35. Detailed Interconnections and Capacitor Recommendations

APPLICATION INFORMATION

12-V flash memory supply

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 36, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 µA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference, pin 2 of TPS6734, is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).



† Not on SNP2x41

NOTE A: The enable terminal can be tied to a general-purpose I/O terminal on the PCMCIA controller or tied high.

Figure 36. SNP2x41 and SNP2x61 with TPS6734 12-V, 120-mA Supply

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SNP2X41APWPRG4	PREVIEW	HTSSOP	PWP	24	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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